CLAIMS

[0054] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor comprising:

a substrate formed over a base layer;

a plurality of pixel cells formed within said substrate, each pixel cell comprising a photo-conversion device; and

a plurality of trenches, each trench being provided along a perimeter of a respective pixel cell, each trench extending to a surface of the base layer, each trench having sidewalls, and being at least partially filled with a material that prevents at least a portion of electrons from passing through said trench.

2. The sensor of claim 1, further comprising a dielectric material formed along at least a portion of said sidewalls.

3. The sensor of claim 2, wherein the dielectric material is an oxide.

4. The sensor of claim 2, wherein the dielectric material is formed on the sidewalls of the trench but not on a bottom of the trench.

5. The sensor of claim 2, wherein the dielectric material comprises at least two materials having different indices of refraction.

6. The sensor of claim, 1 wherein said material is a conductive material.

7. The sensor of claim 6, wherein said conductive material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

8. The sensor of claim 1, wherein said trench has a depth greater than about 2000 Angstroms.

9. The sensor of claim 8, wherein said trench has a depth in the range of about 4000 to about 5000 Angstroms.

10. The sensor of claim 1, wherein the sensor comprises a CMOS image sensor.

11. The sensor of claim 1, wherein the sensor comprises a CCD image sensor.

12. The sensor of claim 1, wherein the pixel cells are red pixel cells of a Bayer pattern.

13. The sensor of claim 1, further comprising a contact adjacent at least one of the plurality of trenches, for biasing the material within the trench positive or negative.

14. A structure for isolating an active area on a semiconductor device, said structure comprising:

a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends to a surface of a base layer below said substrate, and wherein said trench has sidewalls;

a dielectric liner formed along said sidewalls; and

a material formed over said dielectric liner that at least partially fills said trench and prevents at least a portion of electrons from passing through said trench.

15. The structure of claim 14, wherein the dielectric liner comprises an oxide material.

16. The structure of claim 14, wherein the dielectric liner is one of high-density plasma oxide and spin on dielectric oxide.

17. The structure of claim 14, wherein the dielectric liner is formed of a material selected from the group consisting of silicon dioxide, aluminum oxide, undoped polysilicon, silicon nitride, PE-oxide and FSG-oxide.

18. The structure of claim 14, wherein the dielectric liner is formed of at least two materials having different indices of refraction.

19. The structure of claim 14, wherein the dielectric liner is formed of PE-oxide and FSG-oxide.

20. The structure of claim 14, wherein the material is a conductive material.

21. The structure of claim 20, wherein the conductive material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

22. The structure of claim 14, wherein the trench has a depth greater than about 2000 Angstroms.

23. The structure of claim 22, wherein the trench has a depth in the range of about 4000 to about 5000 Angstroms.

24. The structure of claim 14, wherein the semiconductor device comprises one of a CMOS image sensor or a CCD image sensor.

25. The structure of claim 14, further comprising a contact adjacent the trench, for biasing the material within the trench positive or negative.

26. A processing system, said processing system comprising:

a processor;

a semiconductor device;

a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends to a surface of a base layer below said substrate, and wherein said trench has sidewalls;

a dielectric liner formed along said sidewalls; and

a material formed over said insulating liner that at least partially fills said trench and prevents at least a portion of electrons from passing through said trench.

27. The processing system of claim 26, wherein the dielectric liner is an oxide material.

28. The processing system of claim 26, wherein the dielectric liner is one of high-density plasma oxide and spin on dielectric oxide.

29. The processing system of claim 26, wherein the conductive material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

30. The processing system of claim 26, wherein the trench has a depth greater than about 2000 Angstroms.

31. The processing system of claim 30, wherein the trench has a depth in the range of about 4000 to about 5000 Angstroms.

32. The processing system of claim 26, wherein the semiconductor device comprises a CMOS image sensor.

33. The processing system of claim 26, wherein the semiconductor device comprises a CCD image sensor.

34. The processing system of claim 26, wherein the dielectric liner comprises at least two materials having different indices of refraction.

35. The processing system of claim 26, wherein the dielectric liner comprises PE-oxide and FSG-oxide.

36. The processing system of claim 26, wherein the dielectric liner is provided along the sidewalls of the trench but not on a bottom of the trench.

37. A method of forming a structure for isolating areas in a semiconductor device, said method comprising:

forming a trench having sidewalls in a substrate, said trench extending to a surface of a base layer below said substrate; and

at least partially filling said trench with a conductive material.

38. The method of claim 37, further comprising forming a dielectric liner along the sidewalls.

39. The method of claim 38, wherein the dielectric liner is formed of at least two materials having different indices of refraction.

40. The method of claim 38, wherein the dielectric liner comprises an oxide material.

41. The method of claim 38, wherein the dielectric liner is one of high-density plasma oxide and spin on dielectric oxide.

42. The method of claim 37, wherein the conductive material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

43. The method of claim 37, wherein the trench is formed to a depth greater than about 2000 Angstroms.

44. The method of claim 42, wherein the trench is formed to a depth in the range of about 4000 to about 5000 Angstroms.

45. The method of claim 37, wherein the semiconductor device is part of a color filter array.

46. The method of claim 45, wherein the semiconductor device is part of a Bayer pattern.

47. The method of claim 37, wherein the semiconductor device comprises a CMOS image sensor.

48. The method of claim 37, wherein the semiconductor device comprises a CCD image sensor.